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10/675,776	09/30/2003	Jimmie Earl DeWitt JR.	AUS920030481US1	6262

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mrv

Office Action Summary	Application No.	Applicant(s)	
	10/675,776	DEWITT ET AL.	
	Examiner	Art Unit	
	Tuan A. Vu	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6 and 26-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6 and 26-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the Applicant's response filed 11/01/07.

As indicated in Applicant's response, claims 1-2 have been amended; claims 3-5, 7-25 canceled; and claims 26-48 added. Claims 1-2, 6, 26-48 are pending in the office action.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6, 21, 25 of copending Application No. 10/675777 (hereinafter '777).

Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per instant claims 1, 32, 41, '777 claims 6, 21, 25 also recite determining for a instruction during execution for a association of an indicator associated with receiving a bundle or instruction in a instruction cache; associating a counter based on such determination and incrementing a counter in response to the indicator association with the instruction or event associated with the indicator. The event counting and instruction cache as recited by '777 are construed as obvious representation to a runtime indicator (leading to a counter increment, in which incrementing is count of number of instructions execution) and sending from the cached instruction for execution of the instant claims.

4. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2, 10, 20 of copending Application No. 10/675778 (hereinafter '778). Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following observations.

As per claims 1, 32, 41, '778 claims 2, 10, 20 recite receiving a instruction with an indicator generated from a instruction cache, wherein upon determining that an indicator is associated with an instruction and a signal from the cache instruction, incrementing the counter each time the instructions is executed based on said cache signal. Even though '778 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, this limitation of instruction associated with indicator from cache would made the sending a obvious step within runtime based on instruction being cached in view of the above association and counting event.

5. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 3, 17 of copending Application No. 10/675872 (hereinafter '872).

As per instant claims 1, 32, 41, '872 claims 3, 17 also recite instruction to be monitored and sent from cache instruction, determining whether an instruction in execution is related with an runtime range 'indicator'; and counting each event associated with the instruction if the instruction is associated with that range indicator. Even though '872 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '872 explicitly recites that the indicator is a location within contiguous range, this location-within- range limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing in terms of count of number of instructions execution) in view of the above association determination.

6. Claims 6, 34, 43 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 4, 12, 20 of copending Application No. 10/675721 (hereinafter '721).

As per instant claims 6, 34, 43, '721 claims 4, 12, 20 also recite determining for a instruction during execution for a association of a indicator, shadow memory (Note: even though '721 does not recite counter in shadow memory per se, a set of indicators being sent for

monitoring would have made the counter as obviously in the shadow memory); incrementing a counter in response to the indicator association with the instruction, and responsive to which, executing while incrementing said executing. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '721 does not recite receiving bundle into a instruction cache and sending the received bundle for execution, said limitation of instruction with associated indicator would made the instruction cache receiving and sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. The instruction in the *routine of interest* as recited by '721 is construed as obvious representation to a runtime instruction that requires some action (e.g. to monitor or to trace/modify leading to a counter increment in which incrementing is in terms of count of number of executions) of the instant claims.

7. Claims 1, 32, 41 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 12, 23 of copending Application No. 10/682385 (hereinafter '385).

As per instant claims 1, 32, 41, '385 claims 1, 12, 23 also recite executing instructions and detecting indicators that specify counting of events associated with the executing (Note: even though '385 recites data values in memory specifying counting event, a runtime event such as those memory indicators can be analogous to on runtime indicator of the instant claim); and counting each event associated with indicators. At the time the invention was made, expediting execution using instruction cache associated with profiling was known concept. Even though '385 does not recite receiving bundle into a instruction cache and sending the received bundle for

execution, said limitation of executing instructions associated with indicators would made the instruction cache reception and the sending obvious steps within runtime based on instruction being cached in view of the above known concept, and the incrementing responsive to association of instruction with the indicator. Even though '385 explicitly recites that counting events associated with execution based on detection of value indicators, this limitation would be a obvious representation of any runtime indicator that would characterizes as an event deemed for the counter to be incremented (in which incrementing is in terms of count of number of executions) in view of the above association determination.

Specification

8. The disclosure is objected to because of the following informalities: The disclosed 'instruction cache' amounts to a language that cannot be accepted fdue some lexicographic inconsistency, in regard to one of ordinary skill in the useful arts. The disclosure describes functionality being performed by this 'instruction cache', and that appears non-commensurate with known concept, especially when this functionality is not provided with implementation specifics in the Disclosure that would reasonably confirm that a cache is not solely a storage entity but possesses processing intelligence with it. That is, the Specifications teaches 'when instruction cache 300 determines that ... '(pg. 23, middle); 'process ... Figure 11 ... implemented in an instruction cache' (pg. 32, top); 'process ... Figure 12 ... implemented ... in an instruction cache' (pg. 33, middle); '... implemented in an instruction cache'(pg. 34, 2nd para), while the Disclosure is devoid of hardware or software in combination to corroborate to the fact that 'instruction cache' suddenly seems endowed with functionality of a processor, and according to known concept, this functionality without proper enabling support features, cannot

be accepted, because cache is merely for storage of data or instructions just as memory is for read and write. The 'instruction cache' described as a functional capacity (from the above cited portions) therefore appears a far-fetched feature that cannot be construed as a specific feature that is possessed or invented by this Application, when commonly accepted meaning has it that 'instruction cache' cannot exceed the connotation of a memory capacity; unless this cache is redefined by the Inventor to enable a proper understanding and recognition. Without which redefinition, that 'instruction cache' remains just for storage. The language as disclosed above amount to a language without specific and corroborated implementation facts; and what appears to be processor intelligence capacity from the disclosed 'instruction cache' is deemed not truly enabled.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 1-2, 6, 26-48 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Where applicant acts as his or her own lexicographer to specifically define a term of a claim contrary to its ordinary meaning, the written description must clearly redefine the claim term and set forth the uncommon definition so as to put one reasonably skilled in the art on notice that the applicant intended to so redefine that claim term. *Process Control Corp. v. HydReclaim Corp.*, 190 F.3d 1350, 1357, 52 USPQ2d 1029, 1033 (Fed. Cir. 1999). The term

"instruction cache" in claims 1, 32, 41 is used by the claim to mean "for receiving and for sending" while the accepted meaning is "special memory range or subsystem" (as in RAM) for storing of frequently accessed instructions. The term is indefinite because the specification does not clearly redefine the term. When interpreted in light of the Disclosure for *determining* and *sending* (see Specifications Objection), the above claim language amounts to a lack of enablement impropriety, and an indefinite limitation that would enable one of ordinary skill in the art to make use of the Application.

All the claims dependent from the above base claims (2, 6, 27-40, 42-48) are also indefinite in not remedying to the above impropriety.

The indefinite language above will be treated as though the 'instruction cache' is a single unit (in software and/or hardware form) to receive, determine, enable some monitoring steps and sending.

Claim Rejections - 35 USC § 101

11. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

12. Claims 32-40 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The Federal Circuit has recently applied the practical application test in determining whether the claimed subject matter is statutory under 35 U.S.C. § 101. The practical application test requires that a " useful, concrete, and tangible result" be accomplished. An "abstract idea" when practically applied is eligible for a patent. As a consequence, an invention, which is eligible for patenting under 35 U.S.C. § 101, is in the "useful arts" when it is a machine, manufacture, process or composition of matter, which produces a concrete, tangible, and useful result. The test for practical application is thus to determine whether the claimed invention produces a "useful, concrete and tangible result".

The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101. <http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Specifically, claim 32 recites a computer readable medium; and according to the Specifications (pg. 64, bottom) the medium can be *wireless* links transmission type media, thus not a tangible apparatus or article of manufacture. Hence, this product cannot be construed as a tangible product that would be acceptable as one of the 4 enumerated statutory categories. This deficiency, in consequence, would not fulfill the basic requirement of a real-world application result as set forth in the above. The claim is rejected for being a non-statutory subject matter.

Claims 33-40 are also rejected for not remedying to the above non-statutory category deficiency.

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1-2, 6, 26-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gover et al., USPN: 5,752,062(hereinafter Gover) in view of APA (Admitted Prior Art: Specifications: Description of Related Art, pg. 2-3).

As per claim 1, Gover discloses a method in a data processing system for monitoring execution of instructions, the method comprising:

receiving a bundle, the bundle containing an instruction (e.g. Fig. 1; Fig. 3);

responsive to receiving the bundle, determining whether the bundle contains an indicator, wherein the indicator (see col. 7, lines 15 to col. 7, lines 17) identifies the instruction as one that is to be monitored by a performance monitor unit (Fig. 5);

responsive to a determination that the bundle contains the indicator, incrementing a counter (e.g. Fig. 5; col. 7, line 62 to col. 8, line 17) associated with the instruction wherein the incrementing providing provides a count of a number of times the instruction is executed (see Fig. 6a, 6b); and

sending the bundle to a functional unit for execution of the instruction (col. 4, lines 44-49).

Gover does not explicitly disclose 'instruction cache' unit that *receives the bundle, determine the instruction to be counted based on the indicator for monitoring, and sending the bundle from the ICU to the execution unit*; that is, not implementing the instruction cache, the sequence unit (see Fig. 1) and the monitoring unit (Fig. 2; Fig. 4; col. 7, lines 15 to col. 7, lines 17) in a combined functional unit such as a single instruction cache unit (ICU). Gover discloses bus interface between instruction cache and sequencer unit (see Fig. 1; col. 6, lines 7-20); sequencer unit depending on *rename buffer* interface (col. 6, lines 13-19); dispatching process including associating completion/allocation interfaces (e.g. Fig. 3) for updating information (or indicators) in a reorder buffer in terms of conditions (see *finished, exception* - col. 6, line 66, to col 7, line 2) based on which some monitoring action (e.g. condition 2 - col. 10, line 9-12;

dispatch logic 74 - Fig. 2; col. 7, lines 15 to col. 7, lines 17) can be applied; that is, using the performance monitor unit, in conjunction with the special registers or MMCRn (e.g. Fig. 4; Fig. 5; Fig. 6a). The meta-information being dispatched from the bundle of instructions coming from the reorder buffer, sequencer, rename buffer, and the tight relationship thereof with the original instruction cache (Fig. 1) and the performance monitor by Gover entails that the dispatched bundle contains instructions or data back and forth between cache and hardware monitoring tool. APA teaches combining hardware performance tools (Specifications, pg. 3) into a software application performance system or a trace tool using profiling. In view of the role played by the MMCRn and the sequencer, the cache interface unit, a rename process and the handling of runtime exception based on the hardware monitoring role as in Gover, i.e. the interdependency of functionality (hardware and software) units involved, it would have been obvious for one skill in the art at the time the invention was made to implement Gover's instruction cache, sequencer unit and monitoring unit (*performance monitor 50*, Fig. 4 –i.e. hardware tools) as one functionality called *instruction processing unit* -- or more arbitrarily a 'instruction cache', or ICU- to effectuate a performance monitoring/support functionality such as contemplated by APA in terms of faster hardware performance. That is, one would be motivated to do so because this ICU can be called upon to **receive bundle**, trigger **monitoring event** based on indicators set forth by the reorder buffer inside the sequencer unit and provide expedite monitoring action (based on hardware support) operating on data from the dispatched bundle and based on the dynamic condition/state (e.g. *exception, finished, completion*) indicated by the bundle as set forth above (Fig. 6a, 6b) then accordingly **send the bundle** for execution after the appropriate monitoring action has taken place; and therefore enable the ICU to tackle problem based on state

knowledge, e.g. completed state of an dispatched instructions (see col. 7, line 44 to col 7, line 17; col. 15, line 36 to col. 16, line 22) in a timely manner without delays that would have resulted in cache miss (see col. 16, line 59 to col. 17, line 67)

As per claim 2, Gover discloses resetting the counter if the counter exceeds a threshold value; and reading a value of the counter prior to the counter exceeding the threshold value (e.g. *reset* - col. 12, lines 4-42)

As per claim 6, Gover discloses wherein the counter is located in a shadow memory (col. 8, lines 26-39 – Note: special registers and PMCs with state or content – MMCRn -- maintained via special privilege access mode and being kept in parallel with execution scheduling – see col. 11, lines 14-50 -- as informational support thereof, hence reads on shadowing type of information kept in memory; see SSR col. 9 lines 36-57).

As per claim 26, Gover does not explicitly disclose comprising using a spare field in the bundle to contain the indicator; but based on the indicators received by the execution unit sent by the sequencer and based on which to execute some needed performance monitoring action (see Fig. 6a-b), it would have been obvious for one skill in the art at the time the invention was made to enable a special field in the bundle as set forth in claim 1 so that a spare slot contains this indicator, among the other slots that are primarily allotted for the instruction per se (see Fig. 3)

As per claim 27-28, Gover discloses responsive to a determination that the bundle contains the indicator, sending a signal to the performance monitor unit (interrupt - col. 9, lines 30 to col. 10, line 5; Fig. 7); wherein the step of incrementing the counter (e.g. col. 10, lines 40-63) associated with the instruction is performed by the performance monitor unit.

As per claim 29, Gover discloses responsive to a determination that the bundle contains the indicator, beginning incrementing the counter, wherein the counter (refer to claim 27-28) tracks any subsequent instruction executed by an associated processor (e.g. *to correspond to a particular processor* – col. 8, lines 46-55).

As per claims 30-31, Gover does not disclose receiving a second bundle at the instruction cache; responsive to receiving the second bundle, determining whether the second bundle contains a second indicator; and responsive to a determination that the second bundle contains the second indicator, ending incrementing the counter. But the ICU for receiving, determining responsive to an indicator has been addressed in claim 1; and in light of the subsequent incrementing for monitoring an event (see claim 29), Gover discloses wherein the counter and the second counter are identical. For the second indicator, however, based on the providing of stop point in the hardware monitoring registers as by Gover (*stop point* – col. 10, lines 1-16; *threshold value* – col. 10, lines 40-66) where some indicators can be adjusted, it would have been obvious for one skill in the art at the time the invention was made to implementing monitoring unit by Gover so that when a second bundle contains a stop point or a threshold being reached or exceeded, some counting would have to be stopped for an corrective action to take place.

As per claim 32, Gover discloses computer program product comprising:
a computer readable medium having computer useable program code for monitoring execution of instructions, the computer program product comprising code for performing the steps of:

receiving a bundle…;

determining whether ...indicator ...;

incrementing ... ;

sending ... for execution;

all of which have been addressed in claim 1, incorporating thereby the rationale as to render the 'instruction cache' (for receiving determining incrementing and sending) limitation obvious as set forth therein.

As per claims 33-34, refer to claims 2, 6 respectively.

As per claims 35-40, refer to claims 26-31, respectively.

As per claim 41, Gover discloses a data processing system comprising:

a bus; a communications unit connected to the bus; a storage device connected to the bus, wherein the storage device includes computer usable program code; and a processor unit connected to the bus (Fig. 1), wherein the processor unit executes the computer usable program code to:

receive a bundle...;

determine whether ...indicator ...;

increment ... ;

send ... for execution; all of which have been addressed in claim 1, incorporating thereby the rationale as to render the 'instruction cache' (for receiving determining incrementing and sending) limitation obvious as set forth therein.

As per claims 42-48, refer to claims 33-39, respectively.

Response to Arguments

15. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan A Vu whose telephone number is (571) 272-3735. The examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571)272-3756.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3735 (for non-official correspondence - please consult Examiner before using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-272-3609.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
Patent Examiner,
Art Unit 2193
December 19, 2007